Introduction

The EFL Series power supplies have the unique capability of providing 15 or 30 kilovolts (model dependent) of isolation between the input and output. These power supplies are low-voltage, DC-to-DC converters that provide an isolated 12V or 24V floating power source. The EFL Series also provides analog and digital communications between the input and output circuitry. The communications is accomplished digitally, providing excellent linearity, stability, and low temperature drift with a resolution of 16 bits.

The EFL Series performs all the functions of the FL Series power supply with the addition of several important features. The EFL Series has an additional analog up channel, as well as ‘quiet mode’ and ‘half quiet mode’.

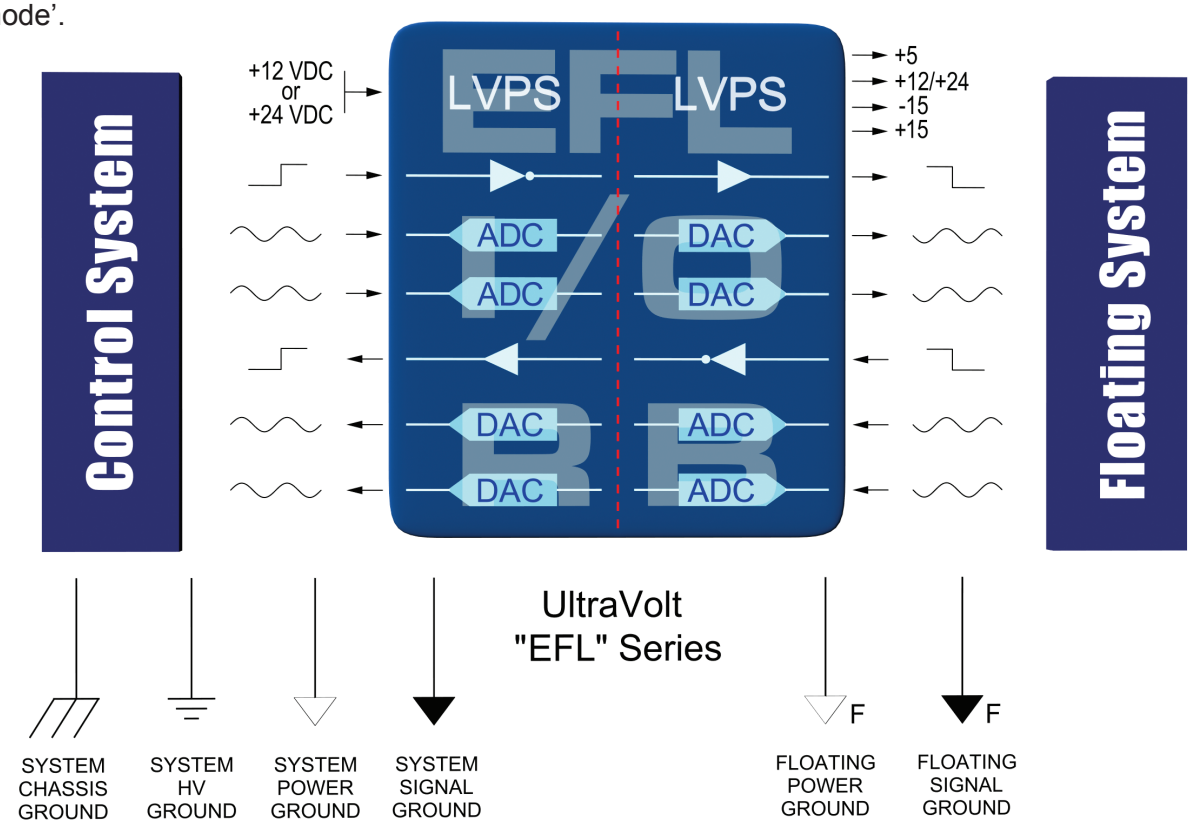

Figure 1: Function Diagram of the EFL Series

Ground-side pin functions

First row pins:

Pin 1, Power Ground: Use this pin for the input power return. Do not allow input-power-return current to flow through the Signal Ground connections. The power ground and signal ground are joined internally. There is no electrical connection between these grounds and the floating grounds.

Pin 2, Input Power: The input voltage on the EFL Series is available at either 12Vdc nominal or 24Vdc nominal. See the EFL Series data sheet for input voltage tolerance.

Pin 3, LVPS Enable/Disable: A voltage between 0V and 0.8V will disable the EFL Series power supply. A voltage between 3.2V and 5V will enable the unit. If the pin is left open, the power supply will default to an enabled state. Grounding the enable/disable pin will disable the unit. The input characteristics can be accurately modeled as a 1kΩ resistor driving the base of a PNP transistor.

Pin 4, TTL up channel input: The TTL up channel is a digital link between the ground-referenced circuitry and the floating circuitry. This channel is commonly used to drive the enable pin on a floating high voltage power supply (HVPS). The output of this digital link is Pin 11 on the floating side. The threshold for the input is logic low between 0V and 0.8V and logic high between 2.4V and 5.0V. The digital links are inverted and have an internal 10kΩ pull up.

Note: *For proper start up of the microprocessor the LVPS Enable/Disable (pin 3) and TTL Up inputs must be driven by an open collector or a pull up resistor with a value greater than 10KΩ.*

Pin 5, Signal Ground: The signal ground and power ground are common inside the power supply. This pin should be used as reference for all analog signals. If input power current is allowed to flow through this pin, offsets can occur which will degrade accuracy.

Pin 6, Analog up channel 1 input: A 0V to +10V for 24V units or 0 to +5V for 12V units signal between this pin and signal ground will result in a 0V to +10V for 24V units or 0 to +5V for 12V units signal on the isolated side of the EFL Series (floating pin 13) that is referenced to the floating signal ground (floating pin 12). There is no direct electrical connection between the analog input signal and the analog output signal. This function is commonly used to provide the remote adjust voltage to a floating HVPS.

Pin 7, +5.1V reference voltage: The internal +5.1V reference is provided for external use through a 464Ω resistor.

Second Row Pins:

Pin 8, Analog down channel 1 output (+): This is the output of one of the analog down communications channels; the input side is on the floating pins. A 0V to 10V for 24V units or 0 to 5V for 12V units signal input on the high-side channel 1 will result in a 0V to +10V for 24V units or 0 to +5V for 12V units signal on this pin with reference to the signal ground on pin 5.

Pin 9, Analog down channel 1 output (-): This pin provides the compliment to the voltage on pin 8. A 0V to 10V for 24V units or 0 to 5V for 12V units signal input on the high-side channel 1 will result in a 0V to -10V for 24V units or 0 to -5V for 12V units signal on this pin with reference to the signal ground on pin 5 corresponding to the voltage on pin 8, but inverted.

Pin 10, Analog down channel 2 output (+): This is the output of one of the analog down communications channels; the input side is on the floating pins. A 0V to 10V for 24V units or 0 to 5V for 12V units signal input on the high-side channel 2 will result in a 0V to +10V for 24V units or 0 to +5V for 12V units signal on this pin with reference to the signal ground on pin 5.

Pin 11, Analog down channel 2 output (-): This pin provides the compliment to the voltage on pin 10. A 0V to 10V for 24V units or 0 to 5V for 12V units signal input on the high-side channel 2 will result in a 0V to -10V for 24V units or 0 to -5V for 12V units signal on this pin with reference to the signal ground on pin 5 corresponding to the voltage on pin 10, but inverted.

Pin 12, Analog up channel 2 input: A 0V to +10V for 24V units or 0 to +5V for 12V units signal between this pin or signal ground will result in a 0V to +10V for 24V units or 0 to +5V for 12V units signal on the isolated side of the EFL Series (floating pin 6) that is referenced to the floating signal ground (floating pin 12). There is no direct electrical connection between the analog input signal and the analog output signal. This function is commonly used to provide the remote adjust voltage to a floating HVPS.

Pin 13, Quiet Mode: The EFL Series uses a digital link to provide the analog communications between the ground side and floating side that has a 16-bit resolution. In applications that are sensitive to noise and variations on the analog output, the quiet mode is used to latch the output DAC and prevent bit jumping. ½ quiet mode latches the up channels, and full quiet mode will latch both up and down channels. The digital up and down links work normally regardless of the quiet-mode status.

The mode pin has an internal 20kΩ pull down resistor; the default condition if this pin is left open is normal operation. The following thresholds apply:

Normal operation:	0V to 0.8V
Full Quiet Mode:	3.0V to 5.6V
½ Quiet Mode:	-9.0V to -4.0V

Pin 14, TTL down channel output: This pin is the output of the TTL down channel. The logic is inverted. A low level input is 0V to 0.55V; a high is from 3.8V to 5.0V. This pin can sink 3mA maximum and source 1mA maximum.

Floating-side pin functions

First row pins (outside pins):

Pin 8, Floating Power Ground: Use this connection as the return for the floating output voltage. This pin is joined internally to the Floating Signal Ground. There is no electrical connection between these grounds and the low-side grounds.

Pin 9, Floating output power (+12V or +24V): his is the main output voltage for the EFL Series DC-to-DC converter. This voltage output is commonly used as the main input power to a floating HVPS or filament power supply, such as the UltraVolt FIL Series. Use pin 8 for the power return.

Pin 10, Floating -15V output: This is a low-current, -15V fixed output. This voltage is commonly used as the negative rail on operational amplifiers and other analog circuitry. See the EFL Series data sheet for maximum current draw and voltage tolerance.

Pin 11, Floating TTL Up output: This pin is the output of the TTL up channel. The logic is inverted. A low level input is 0V to 0.55V; a high is from 3.8V to 5.0V. This pin can sink 3mA maximum and source 1mA maximum.

Pin 12, Floating Signal Ground: The floating signal ground and floating power ground are common inside the power supply. This pin should be used as reference for all floating analog signals. If output power current is allowed to flow through this pin, offsets can occur which will degrade accuracy.

Pin 13, Floating Analog up channel 1 out: This is the output of the analog up channel 1 communications channel; the input is on the ground-side pins. A 0V to +10V for 24V units or 0 to +5V for 12V units signal on the input at Pin 6 on the ground side will result in a 0V to +10V for 24V units or 0 to +5V for 12V units signal on this pin with reference to the floating signal ground on pin 12.

Pin 14, Floating +5.1V output: An internal +5.1V source is provided for external use. Please see the EFL Series data sheet for current capacity.

Pin 1, Floating Analog Down (+) Input 1: This pin is the non-inverting input of a differential amplifier. A 0V to 10V for 24V units or 0 to 5V for 12V units signal between (-) input 1 and (+) input 1 will cause a 0V to 10V for 24V units or 0 to 5V for 12V units signal on the ground-referenced side along with its compliment on Pin 8 and Pin 9.

Pin 2, Floating Analog Down (-) Input 1: This is the inverting input of a differential amplifier referenced above on Pin 1.

Pin 3, Floating Analog Down (+) Input 2: This pin is the non-inverting input of a differential amplifier. A 0V to 10V for 24V units or 0 to 5V for 12V units signal between (-) input 2 and (+) input 2 will cause a 0V to 10V for 24V units or 0 to 5V for 12V units signal on the ground-referenced side along with its compliment on Pin 10 and Pin 11.

Pin 4, Floating Analog Down (-) Input 2: This is the inverting input of a differential amplifier referenced above on Pin 3.

Pin 5, +15V output: This is a low-current, +15V fixed output. This voltage is commonly used as the positive rail on operational amplifiers and other analog circuitry. See the EFL Series data sheet for maximum current draw and voltage tolerance.

Pin 6, Floating Analog up channel 2 out: This is the output of the analog up channel 2 communications channel; the input is on the ground-side pins. A 0V to +10V for 24V units or 0 to +5V for 12V units signal on the input at Pin 12 on the ground side will result in a 0V to +10V for 24V units or 0 to +5V for 12V units signal on this pin with reference to the floating signal ground on Pin 12.

Pin 7, Floating TTL down input: The TTL down channel is a digital link between the floating-referenced circuitry and the ground-side circuitry. The output of this digital link is Pin 14 on the ground side. The threshold for the input is logic low between 0V and 0.8V and logic high between 2.4V and 5.0V. The digital links are inverted, and have an internal 10kΩ pull up.

Note: *For proper start up of the microprocessor the Floating TTL Down input must be driven by an open collector or a pull up resistor with a value greater than 10KΩ.*